FIG. 1

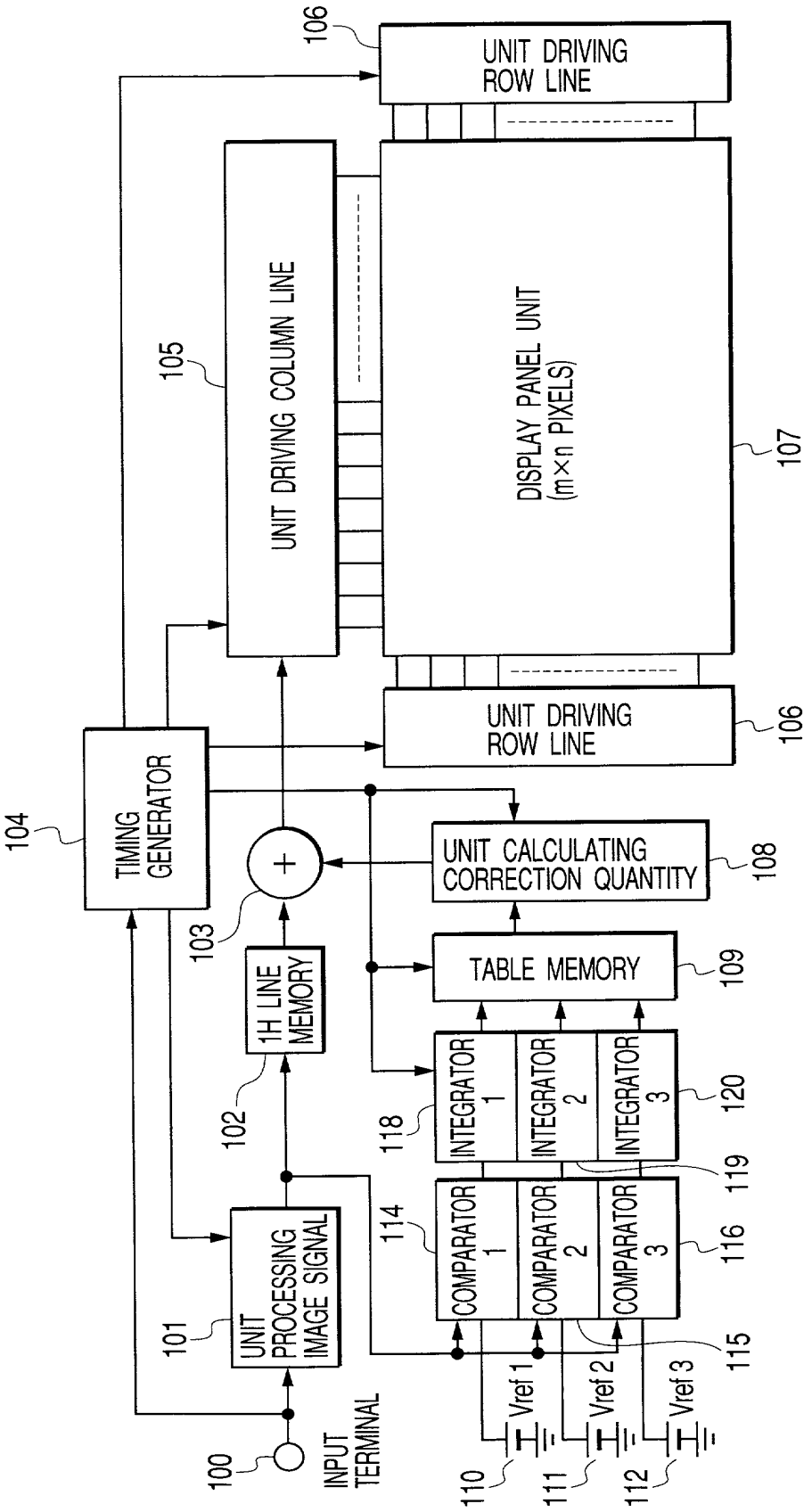

106
UNIT DRIVING ROW LINE
105
UNIT DRIVING COLUMN LINE
DISPLAY PANEL UNIT (m×n PIXELS)
107
UNIT DRIVING ROW LINE
106
104
TIMING GENERATOR
103
UNIT CALCULATING CORRECTION QUANTITY
108
TABLE MEMORY
109
1H LINE MEMORY
102
INTEGRATOR 1
INTEGRATOR 2
INTEGRATOR 3
118
120
119
COMPARATOR 1
COMPARATOR 2
COMPARATOR 3
114
116
115
101
UNIT PROCESSING IMAGE SIGNAL
Vref 1
Vref 2
Vref 3
100
INPUT TERMINAL
110
111
112

FIG. 2

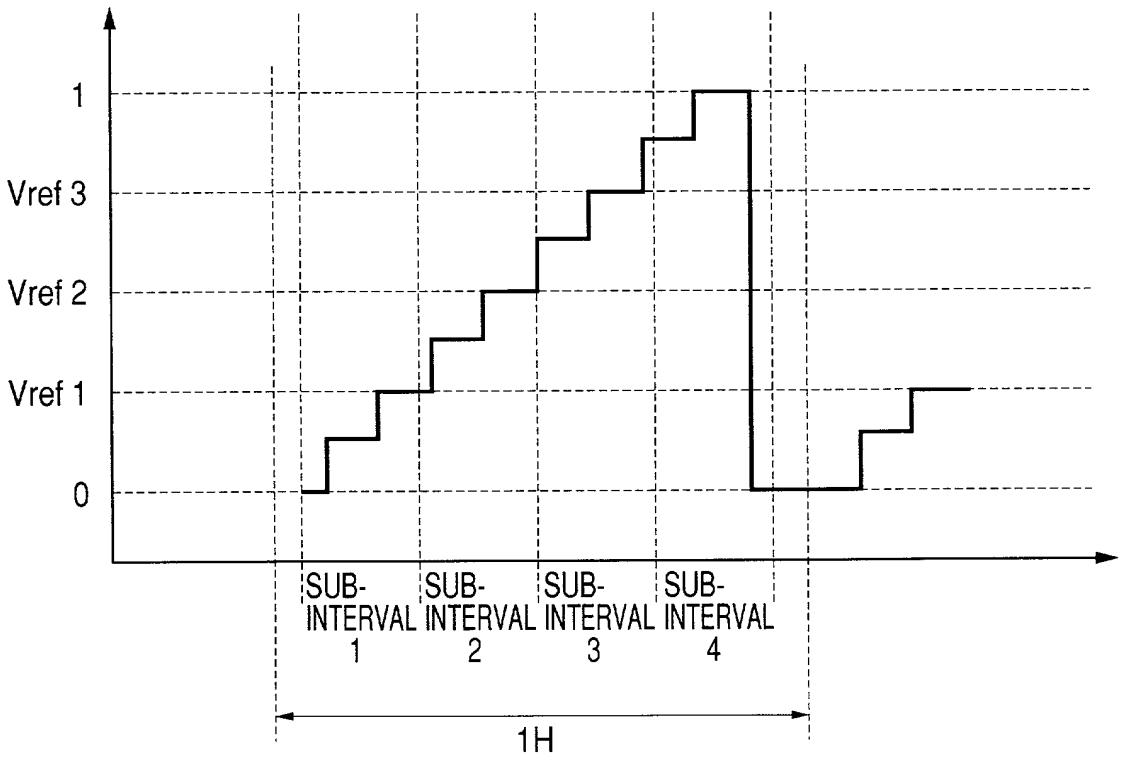

1
Vref 3
Vref 2
Vref 1
0
SUB-INTERVAL 1
SUB-INTERVAL 2
SUB-INTERVAL 3
SUB-INTERVAL 4
1H

FIG. 3

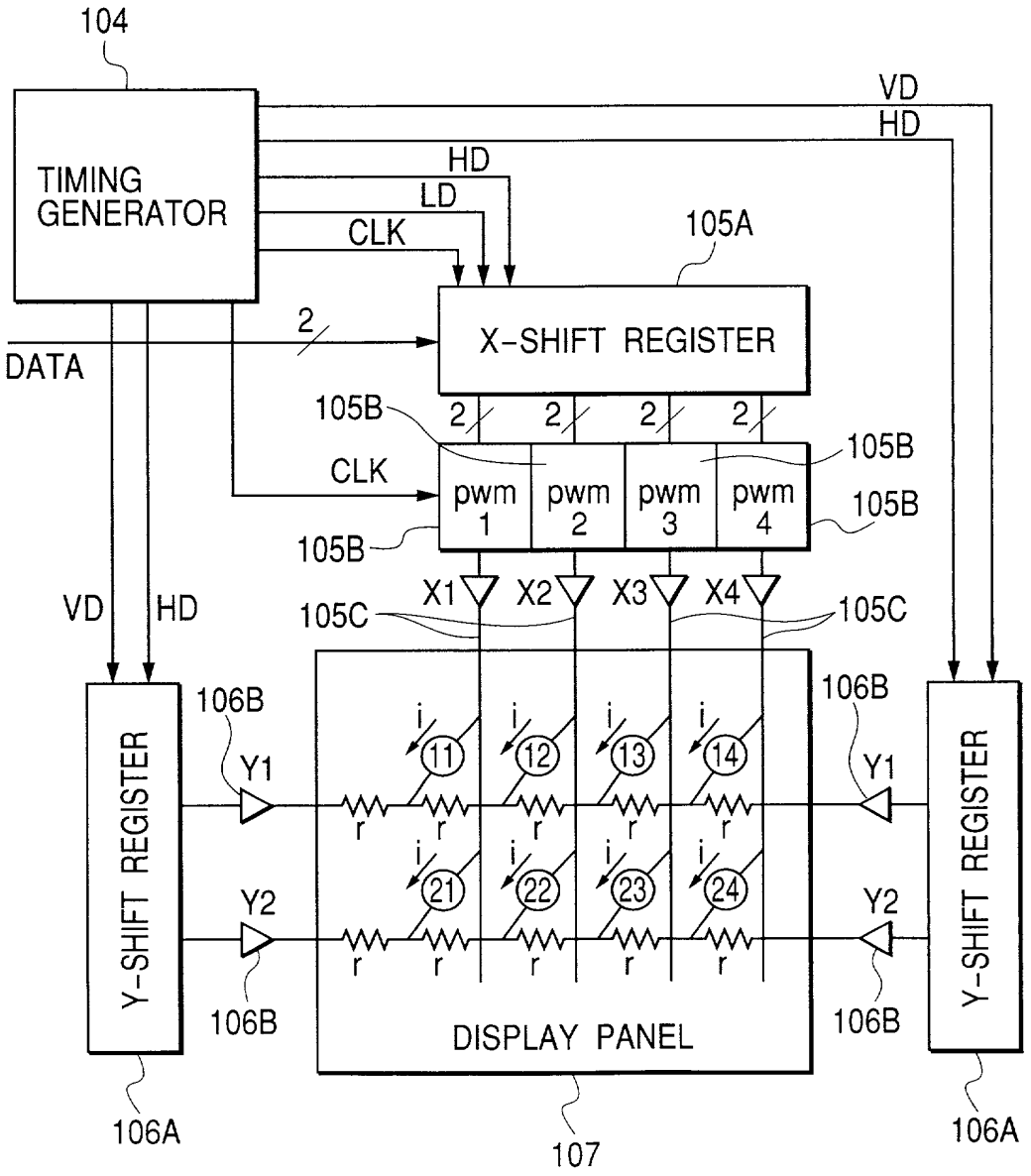
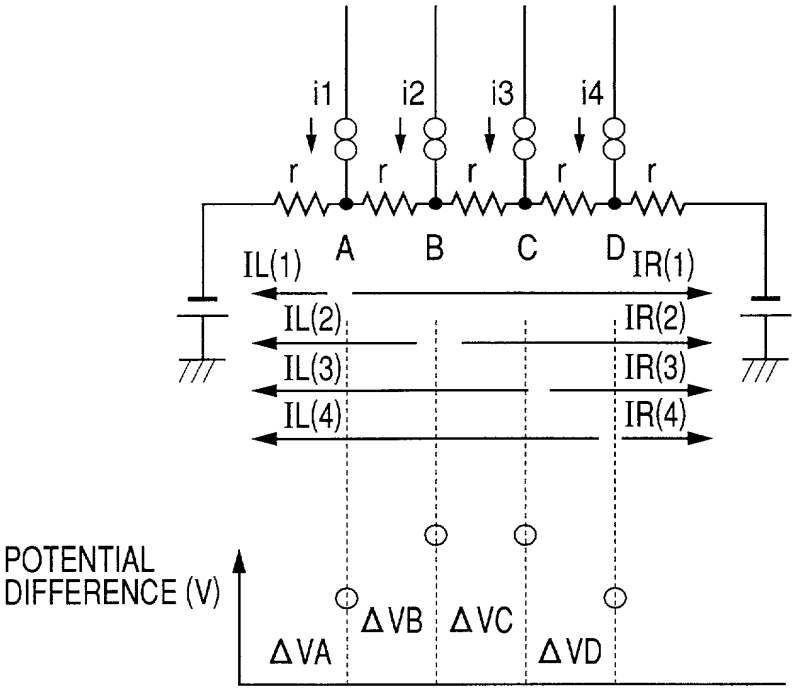

104
TIMING GENERATOR
VD
HD
LD
CLK
105A
X-SHIFT REGISTER
DATA
2
105B
pwm 1
pwm 2
pwm 3
pwm 4
X1
X2
X3
X4
105C
Y-SHIFT REGISTER
106B
Y1
Y2
106A
DISPLAY PANEL
107
r
i
11
12
13
14
21
22
23
24

FIG. 4



$$IL(1)=(r*4/5)*i1 \quad IR(1)=(r*1/5)*i1$$
$$IL(2)=(r*3/5)*i2 \quad IR(2)=(r*2/5)*i2$$
$$IL(3)=(r*2/5)*i3 \quad IR(3)=(r*3/5)*i3$$
$$IL(4)=(r*1/5)*i4 \quad IR(4)=(r*4/5)*i4$$

$$\Delta VA = r * \sum_{k=1}^{4} (IL(k))$$

$$\Delta VB = \Delta VA + r * \left(\sum_{k=2}^{4} (IL(k)) - \sum_{k=1}^{1} (IR(k))\right)$$

$$\Delta VC = \Delta VB + r * \left(\sum_{k=3}^{4} (IL(k)) - \sum_{k=1}^{2} (IR(k))\right)$$

$$\Delta VD = \Delta VC + r * \left(\sum_{k=4}^{4} (IL(k)) - \sum_{k=1}^{3} (IR(k))\right)$$

FIG. 5

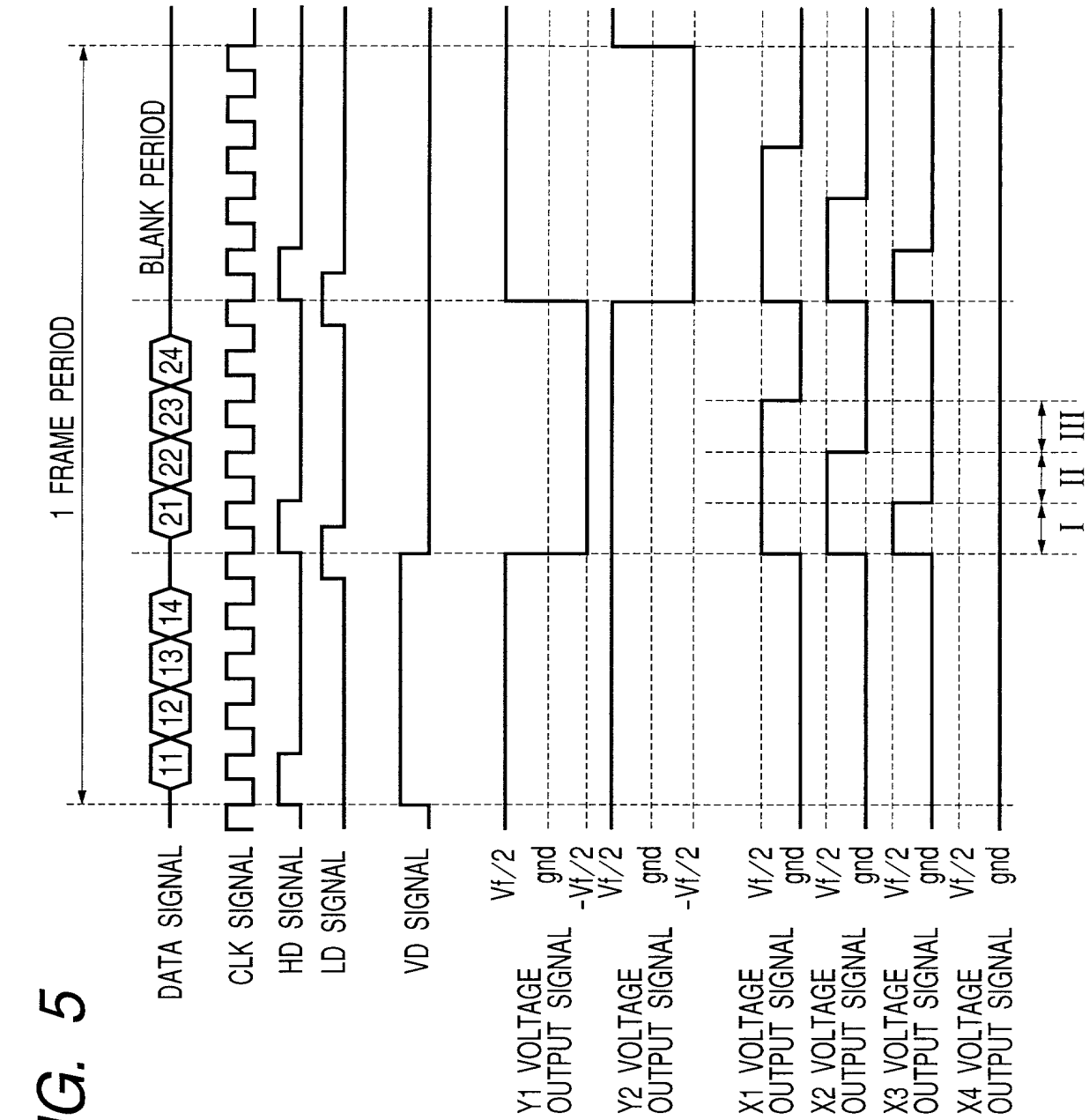

1 FRAME PERIOD
BLANK PERIOD
11
12
13
14
21
22
23
24
DATA SIGNAL
CLK SIGNAL
HD SIGNAL
LD SIGNAL
VD SIGNAL
Y1 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
-Vf/2
Y2 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
-Vf/2
X1 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
X2 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
X3 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
X4 VOLTAGE OUTPUT SIGNAL
Vf/2
gnd
I
II
III

FIG. 6

(1)

	PERIOD I	PERIOD II	PERIOD III
X1 VOLTAGE OUTPUT	ON	ON	ON
X2 VOLTAGE OUTPUT	ON	ON	OFF
X3 VOLTAGE OUTPUT	ON	OFF	OFF
X4 VOLTAGE OUTPUT	OFF	OFF	OFF

(2)

	PERIOD I	PERIOD II	PERIOD III	TOTAL OF ONE HORIZONTAL SCANNING INTERVAL
VOLTAGE DROP AT POINT A	ΔVA(I)	ΔVA(II)	ΔVA(III)	(ΔVA(I)+(ΔVA(II)+(ΔVA(III))/3
VOLTAGE DROP AT POINT B	ΔVB(I)	ΔVB(II)	ΔVB(III)	(ΔVB(I)+(ΔVB(II)+(ΔVB(III))/3
VOLTAGE DROP AT POINT C	ΔVC(I)	ΔVC(II)	ΔVC(III)	(ΔVC(I)+(ΔVC(II)+(ΔVC(III))/3
VOLTAGE DROP AT POINT D	ΔVD(I)	ΔVD(II)	ΔVD(III)	(ΔVD(I)+(ΔVD(II)+(ΔVD(III))/3

FIG. 7

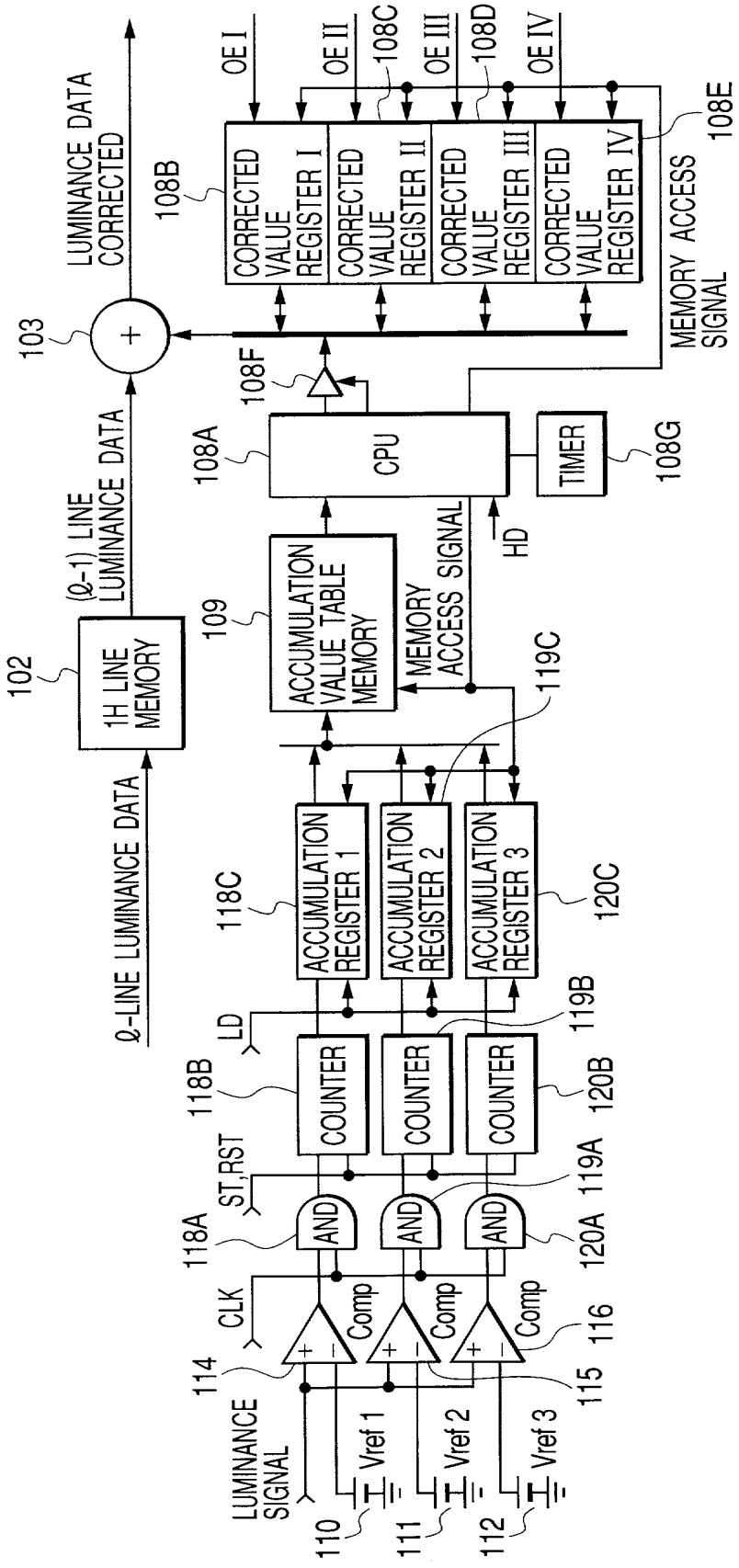

LUMINANCE DATA CORRECTED
103
108B
OE I
OE II
108C
OE III
108D
OE IV
CORRECTED VALUE REGISTER I
CORRECTED VALUE REGISTER II
CORRECTED VALUE REGISTER III
CORRECTED VALUE REGISTER IV
108E
MEMORY ACCESS SIGNAL
108F
(ℓ-1) LINE LUMINANCE DATA
108A
CPU
TIMER
108G
102
1H LINE MEMORY
109
ACCUMULATION VALUE TABLE MEMORY
MEMORY ACCESS SIGNAL
HD
119C
ℓ-LINE LUMINANCE DATA
118C
ACCUMULATION REGISTER 1
ACCUMULATION REGISTER 2
ACCUMULATION REGISTER 3
120C
LD
119B
118B
COUNTER
COUNTER
COUNTER
120B
ST,RST
119A
118A
AND
AND
AND
120A
CLK
Comp
Comp
Comp
116
114
115
LUMINANCE SIGNAL
Vref 1
Vref 2
Vref 3
110
111
112

FIG. 8

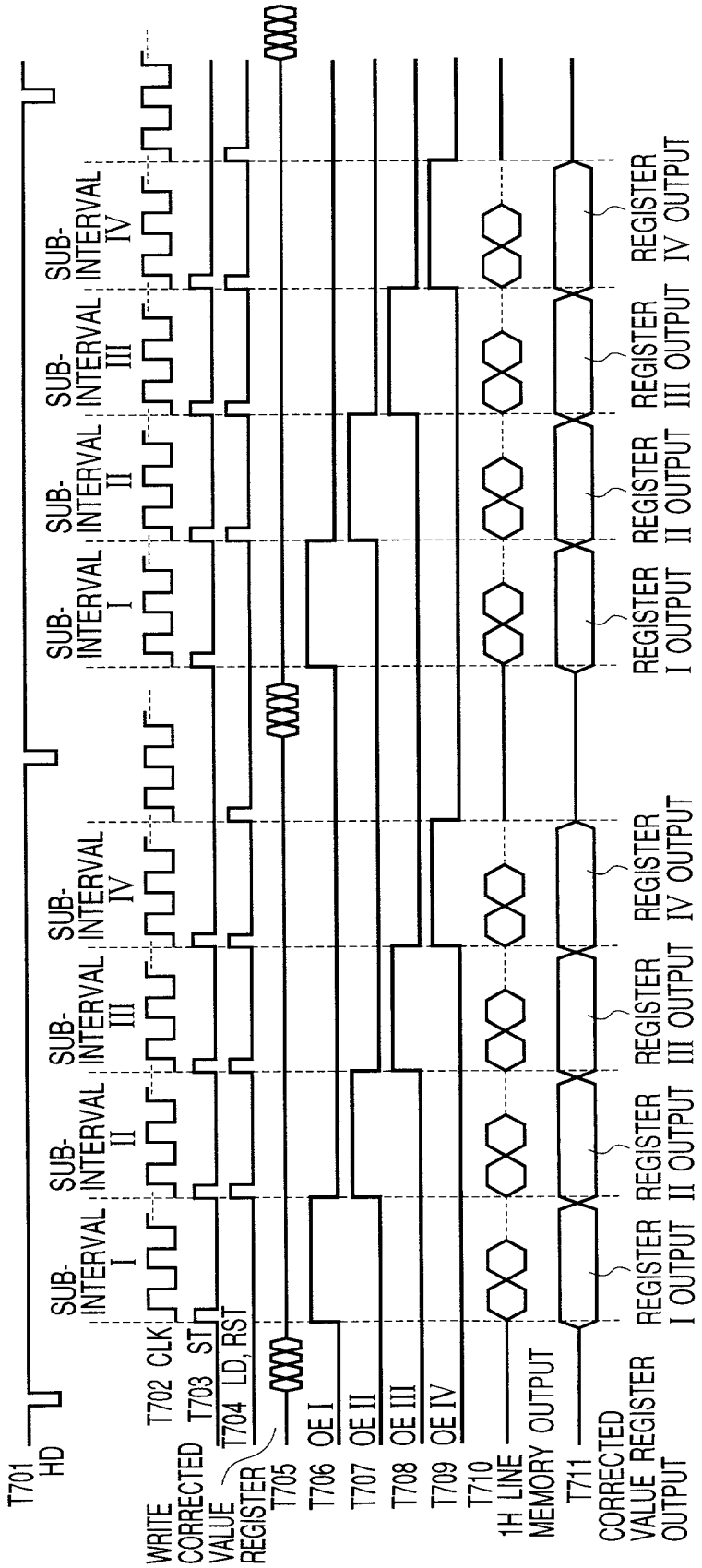

T701
HD
T702 CLK
T703 ST
T704 LD, RST
T705
T706 OE I
T707 OE II
T708 OE III
T709 OE IV
T710
T711
WRITE CORRECTED VALUE REGISTER
1H LINE MEMORY OUTPUT
CORRECTED VALUE REGISTER OUTPUT
SUB-INTERVAL I
SUB-INTERVAL II
SUB-INTERVAL III
SUB-INTERVAL IV
REGISTER I OUTPUT
REGISTER II OUTPUT
REGISTER III OUTPUT
REGISTER IV OUTPUT

FIG. 9

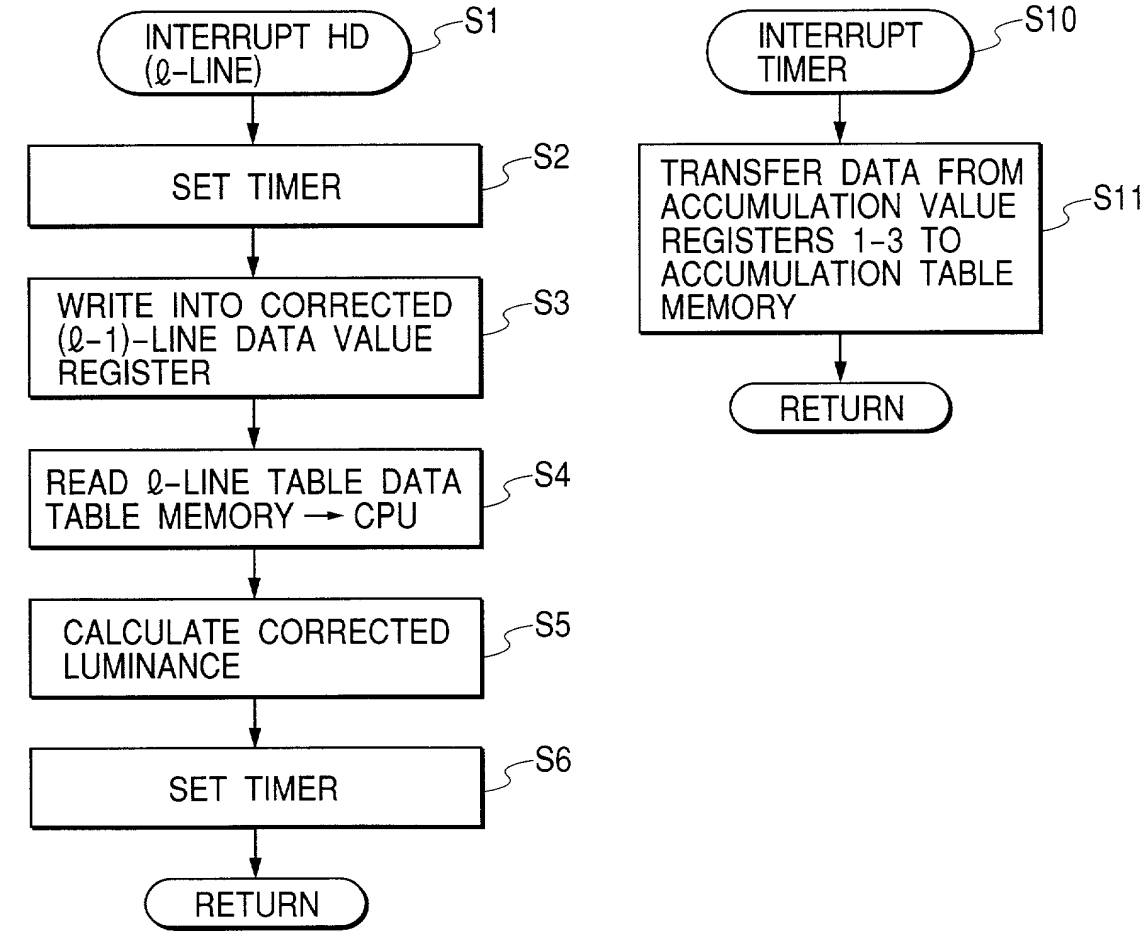

INTERRUPT HD (ℓ-LINE)
S1
SET TIMER
S2
WRITE INTO CORRECTED (ℓ-1)-LINE DATA VALUE REGISTER
S3
READ ℓ-LINE TABLE DATA TABLE MEMORY → CPU
S4
CALCULATE CORRECTED LUMINANCE
S5
SET TIMER
S6
RETURN
INTERRUPT TIMER
S10
TRANSFER DATA FROM ACCUMULATION VALUE REGISTERS 1-3 TO ACCUMULATION TABLE MEMORY
S11
RETURN

FIG. 10

	DATA'S GREATER THAN Vref 1	DATA'S GREATER THAN Vref 2	DATA'S GREATER THAN Vref 3
BLOCK I	NA 1	NA 2	NA 3
BLOCK II	NB 1	NB 2	NB 3
BLOCK III	NC 1	NC 2	NC 3
BLOCK IV	ND 1	ND 2	ND 3

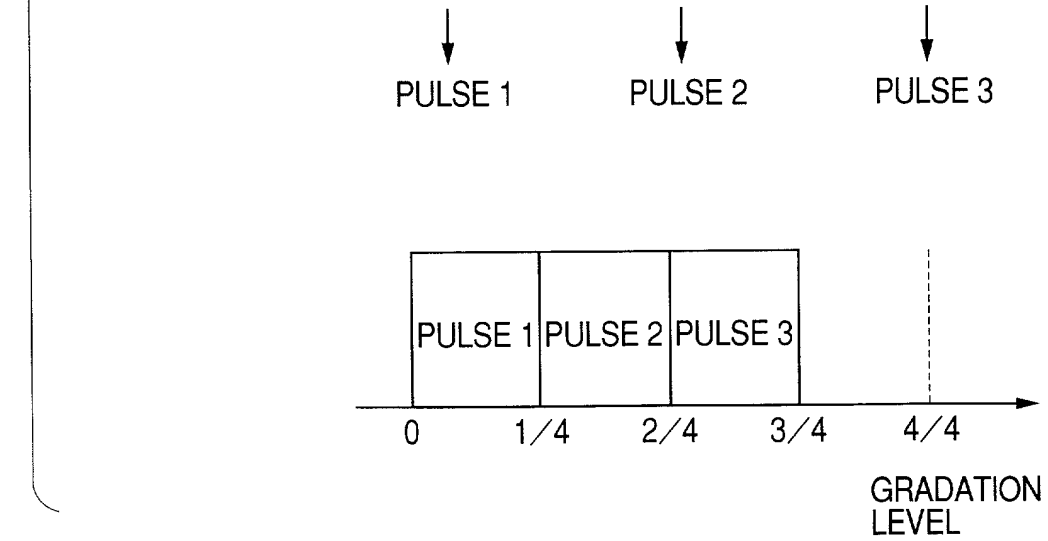


FIG. 11

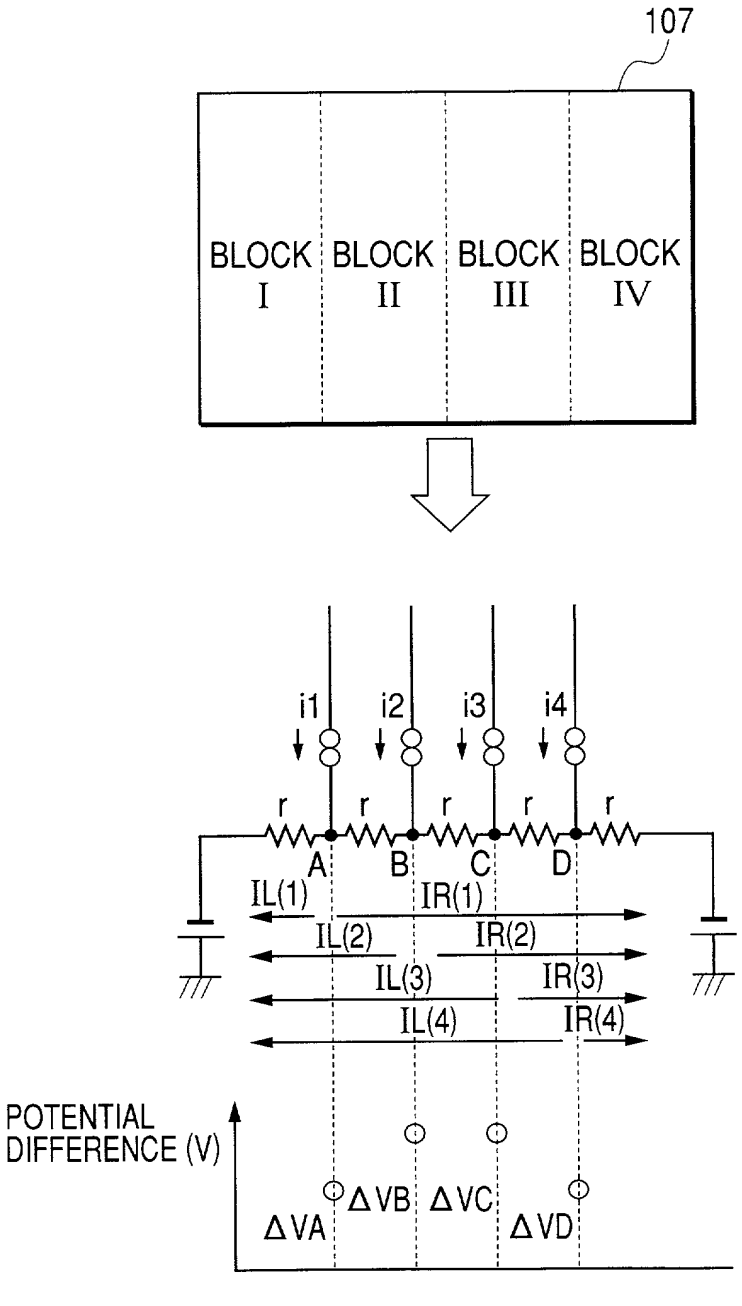

107
BLOCK I
BLOCK II
BLOCK III
BLOCK IV
i1
i2
i3
i4
r
A
B
C
D
IL(1)
IR(1)
IL(2)
IR(2)
IL(3)
IR(3)
IL(4)
IR(4)
POTENTIAL DIFFERENCE (V)
ΔVA
ΔVB
ΔVC
ΔVD

FIG. 12

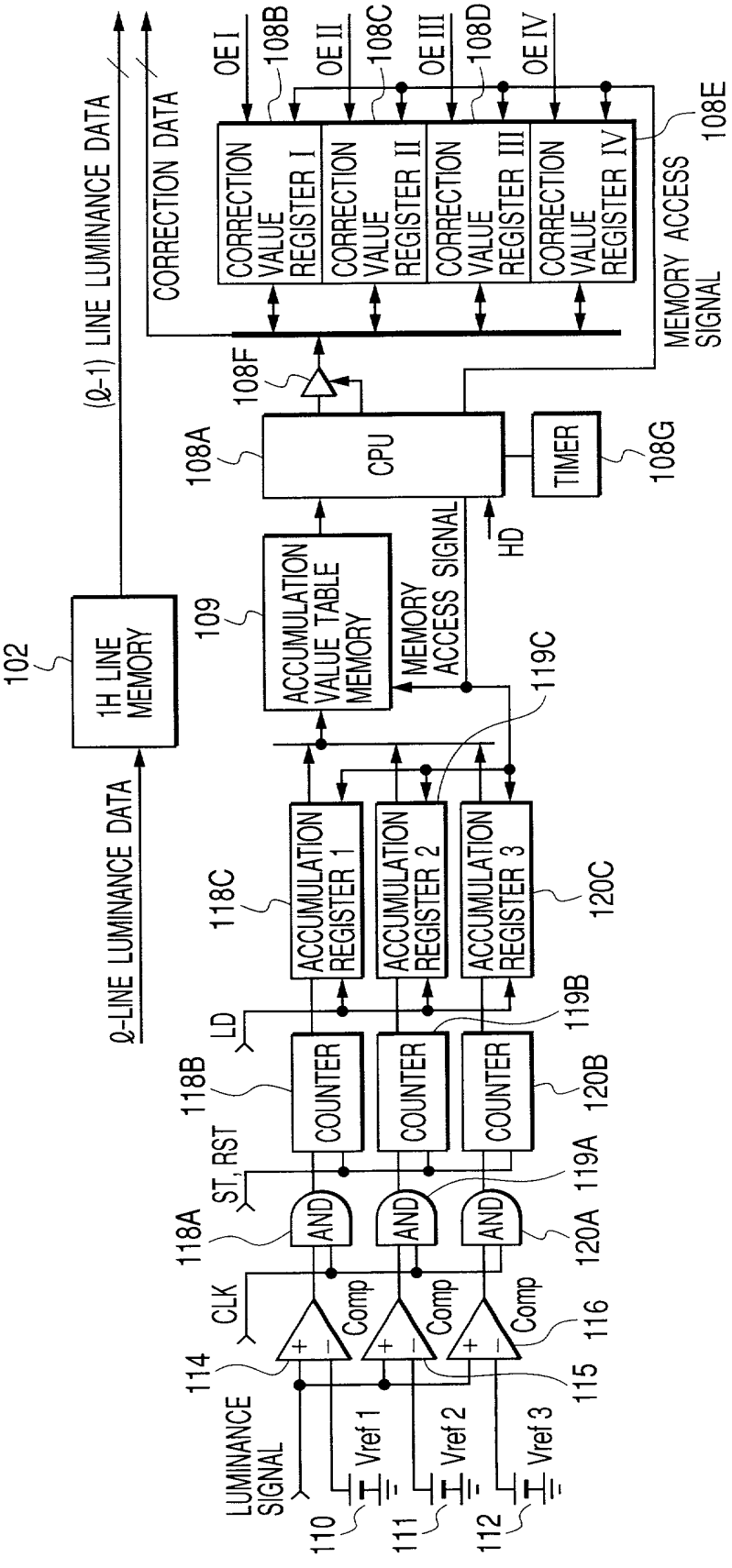

LUMINANCE SIGNAL
Vref 1
Vref 2
Vref 3
110
111
112
114
115
116
CLK
Comp
118A
120A
119A
ST, RST
AND
118B
120B
COUNTER
LD
119B
118C
120C
ACCUMULATION REGISTER 1
ACCUMULATION REGISTER 2
ACCUMULATION REGISTER 3
119C
Ω-LINE LUMINANCE DATA
102
1H LINE MEMORY
(Ω-1) LINE LUMINANCE DATA
109
ACCUMULATION VALUE TABLE MEMORY
MEMORY ACCESS SIGNAL
HD
108A
CPU
108F
TIMER
108G
CORRECTION DATA
OE I
OE II
OE III
OE IV
108B
108C
108D
CORRECTION VALUE REGISTER I
CORRECTION VALUE REGISTER II
CORRECTION VALUE REGISTER III
CORRECTION VALUE REGISTER IV
MEMORY ACCESS SIGNAL
108E

FIG. 13

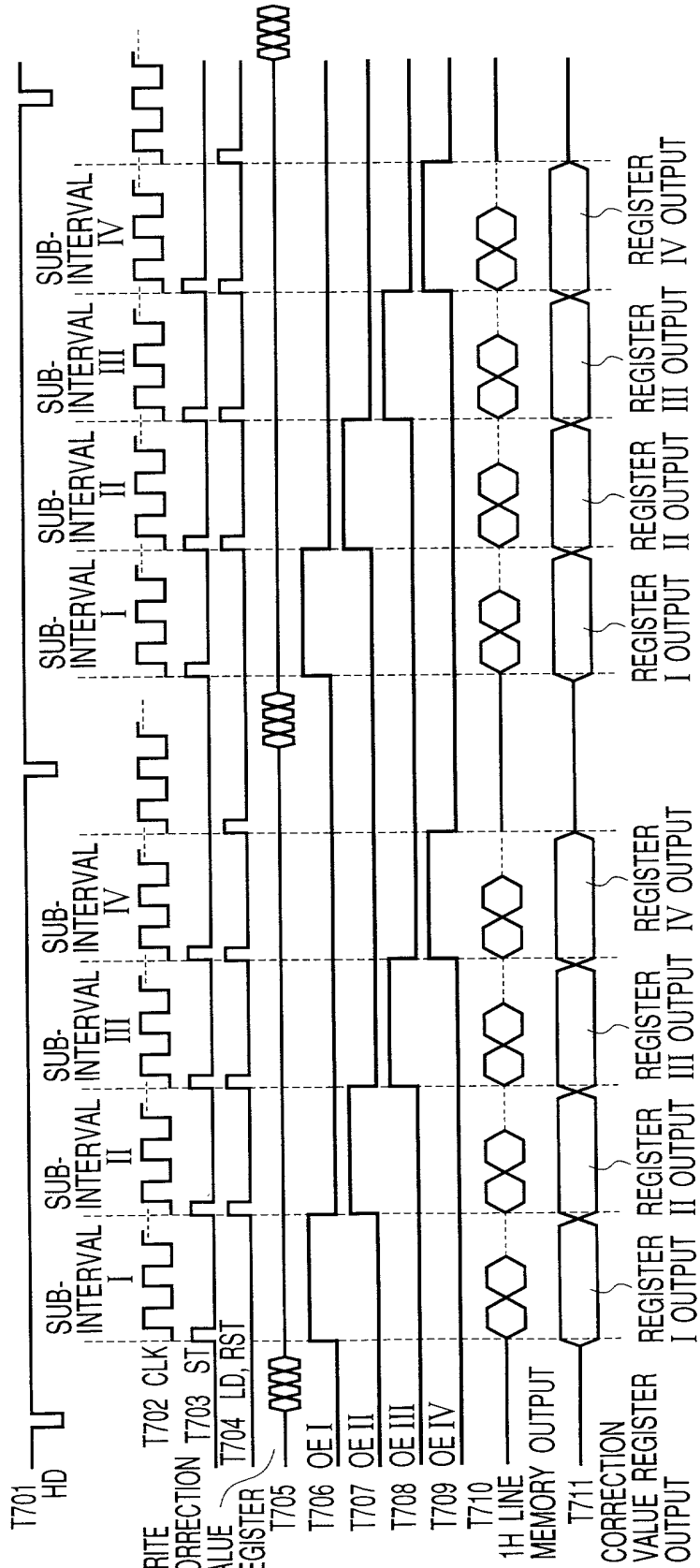

T701
HD
T702 CLK
T703 ST
T704 LD, RST
WRITE CORRECTION VALUE REGISTER
T705
T706 OE I
T707 OE II
T708 OE III
T709 OE IV
T710
1H LINE MEMORY OUTPUT
T711
CORRECTION VALUE REGISTER OUTPUT
SUB-INTERVAL I
SUB-INTERVAL II
SUB-INTERVAL III
SUB-INTERVAL IV
REGISTER I OUTPUT
REGISTER II OUTPUT
REGISTER III OUTPUT
REGISTER IV OUTPUT

FIG. 14

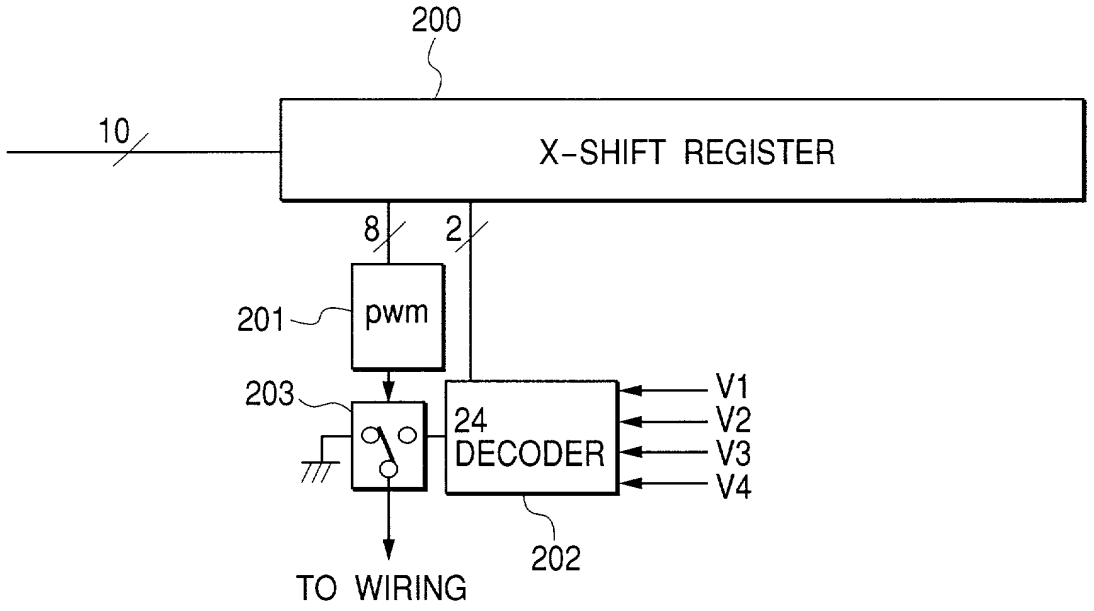


FIG. 15

CORRECTION DATA	OUTPUT
00B	V1
01B	V2
10B	V3
11B	V4

FIG. 16

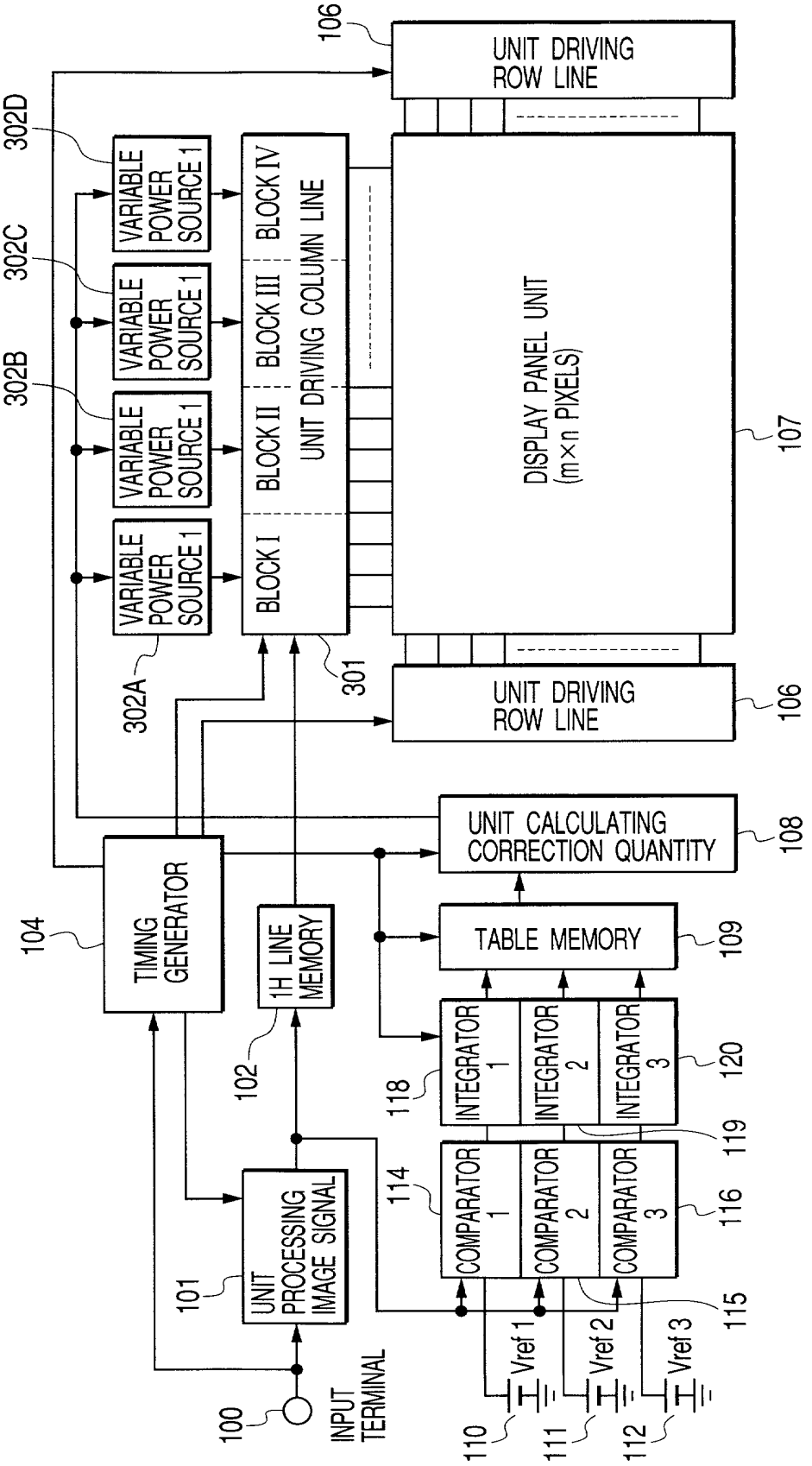
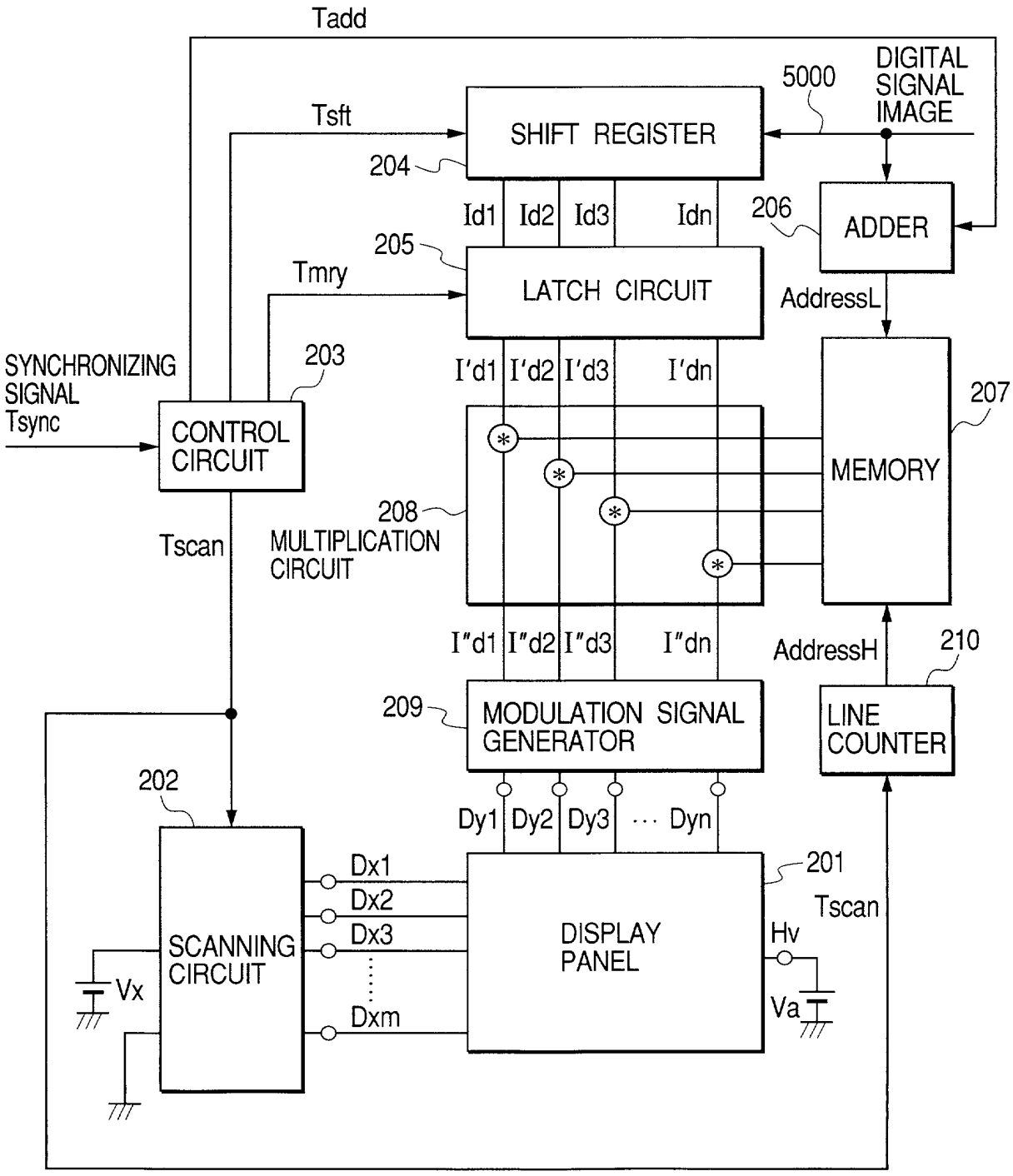

106
UNIT DRIVING ROW LINE
302D
302C
302B
302A
VARIABLE POWER SOURCE 1
BLOCK I
BLOCK II
BLOCK III
BLOCK IV
UNIT DRIVING COLUMN LINE
301
DISPLAY PANEL UNIT (m×n PIXELS)
107
UNIT DRIVING ROW LINE
106
UNIT CALCULATING CORRECTION QUANTITY
108
104
TIMING GENERATOR
1H LINE MEMORY
102
TABLE MEMORY
109
118
INTEGRATOR 1
INTEGRATOR 2
INTEGRATOR 3
120
119
114
COMPARATOR 1
COMPARATOR 2
COMPARATOR 3
116
115
101
UNIT PROCESSING IMAGE SIGNAL
Vref 1
Vref 2
Vref 3
110
111
112
100
INPUT TERMINAL

FIG. 17


Tadd
5000
DIGITAL SIGNAL IMAGE
Tsft
SHIFT REGISTER
204
Id1
Id2
Id3
Idn
206
ADDER
205
Tmry
LATCH CIRCUIT
AddressL
SYNCHRONIZING SIGNAL Tsync
203
I'd1
I'd2
I'd3
I'dn
207
CONTROL CIRCUIT
MEMORY
208
MULTIPLICATION CIRCUIT
Tscan
I"d1
I"d2
I"d3
I"dn
AddressH
210
209
MODULATION SIGNAL GENERATOR
LINE COUNTER
202
Dy1
Dy2
Dy3
Dyn
Dx1
Dx2
Dx3
Dxm
201
Tscan
SCANNING CIRCUIT
DISPLAY PANEL
Hv
Vx
Va